

### Description

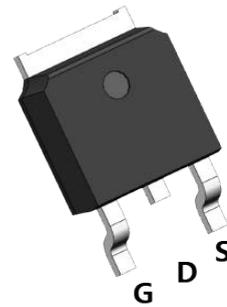
The D80P04 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

### Application

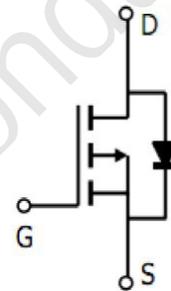
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

### Features

- $V_{DS} = -40V, I_D = -80A$
- $R_{DS(ON)} : 1.5m\Omega @ V_{GS} = 10V$
- Low gate charge.
- Green device available.
- Advanced high cell density trench technology for ultra  $R_{DS(ON)}$
- Excellent package for good heat dissipation.



Marking and pin assignment



P-Channel MOSFET

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	-80	A
Drain Current-Continuous ( $T_C = 100^\circ C$ )	$I_D (100^\circ C)$	-28	A
Pulsed Drain Current	$I_{DM}$	-180	A
Maximum Power Dissipation	$P_D$	73.5	W
Derating factor		0.59	W/ $^\circ C$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	130	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ C$

### Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	1.7	$^\circ C/W$
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**Package Marking and Ordering Information**

Part NO.	Marking	Package
VS4504AD	4504AD	TO-252

**Electrical Characteristics (T<sub>c</sub>=25°C unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	-40	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V	-	-	-1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>On Characteristics (Note 3)</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	-1.0	-1.6	-2.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =10A	-	11.5	15	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =8A	-	16	22	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =20A	-	13	-	S
<b>Dynamic Characteristics (Note 4)</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-25V, V <sub>GS</sub> =0V, F=1.0MHz	-	2757	4000	PF
Output Capacitance	C <sub>oss</sub>		-	240	360	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	137	200	PF
<b>Switching Characteristics (Note 4)</b>						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =20V, I <sub>D</sub> =-1A, V <sub>GS</sub> =-10V, R <sub>G</sub> =6Ω	-	23	40	nS
Turn-on Rise Time	t <sub>r</sub>		-	10	20	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	135	250	nS
Turn-Off Fall Time	t <sub>f</sub>		-	46	90	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-32V, I <sub>D</sub> =10A, V <sub>GS</sub> =-4.5V	-	22.2	40	nC
Gate-Source Charge	Q <sub>gs</sub>		-	8.2		nC
Gate-Drain Charge	Q <sub>gd</sub>		-	8.8		nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =-1A	-		-1	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	-80	A
Reverse Recovery Time	t <sub>rr</sub>		-	-	-	nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	-	-	nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production.
5. EAS condition : V<sub>DD</sub>=25V, V<sub>GS</sub>=10V, L=0.1mH, I<sub>AS</sub>=51A, R<sub>G</sub>=25Ω, Starting T<sub>J</sub>=25°C.

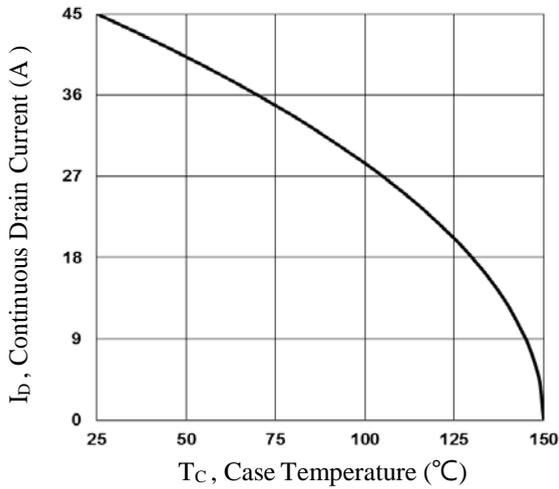


Fig.1 Continuous Drain Current vs.  $T_C$

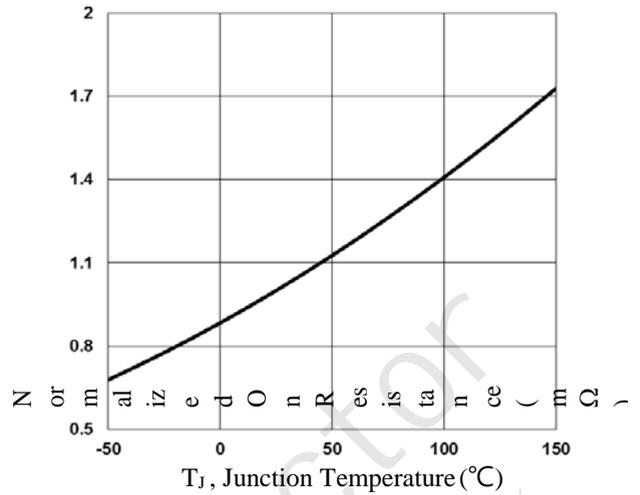


Fig.2 Normalized  $R_{DS(on)}$  vs.  $T_J$

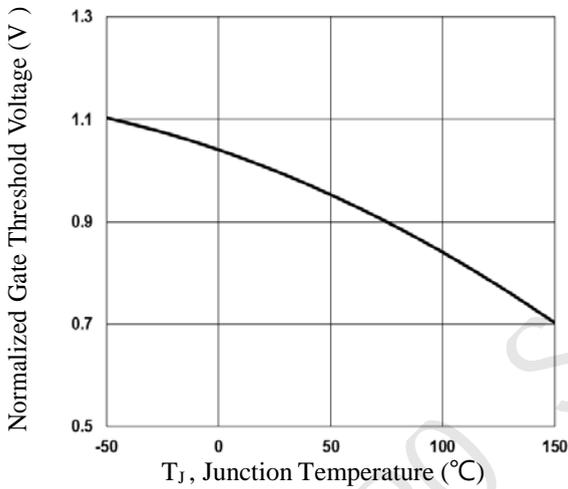


Fig.3 Normalized  $V_{th}$  vs.  $T_J$

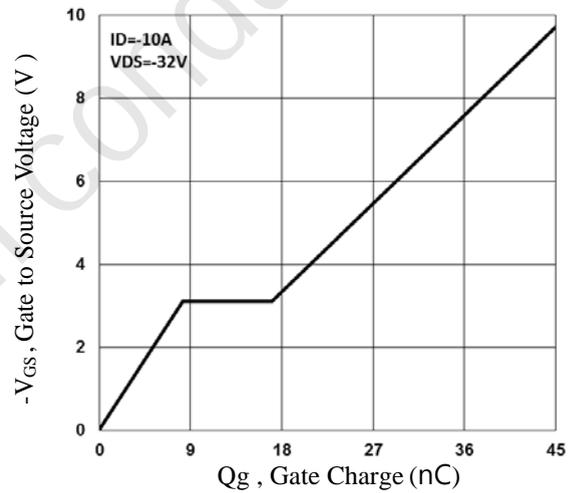


Fig.4 Gate Charge Waveform

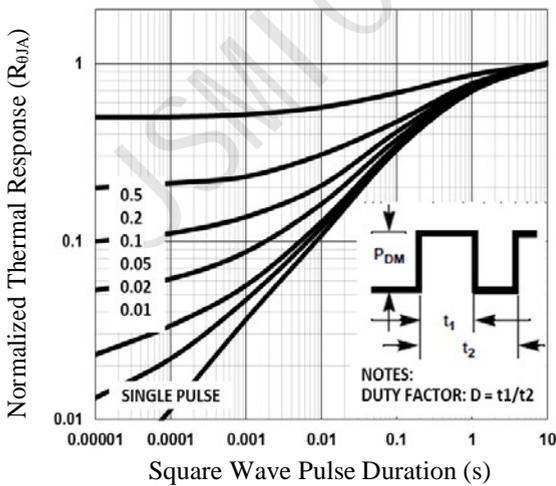


Fig.5 Normalized Transient Impedance

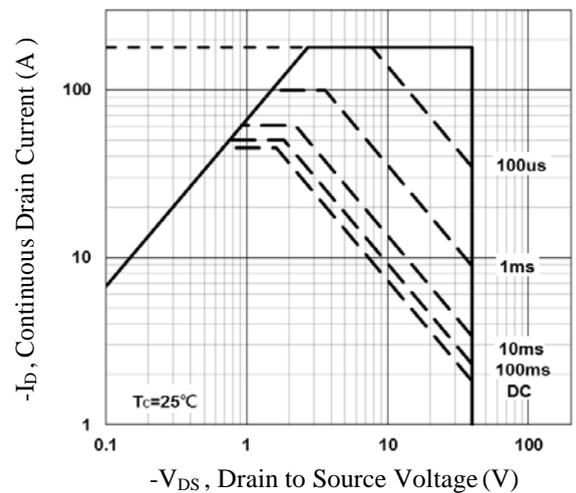


Fig.6 Maximum Safe Operation Area

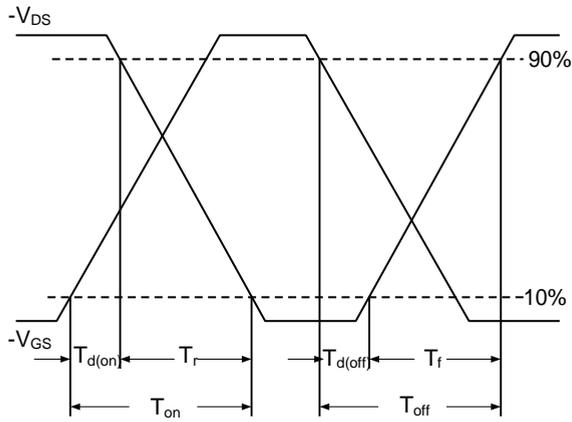


Fig.7 Switching Time Waveform

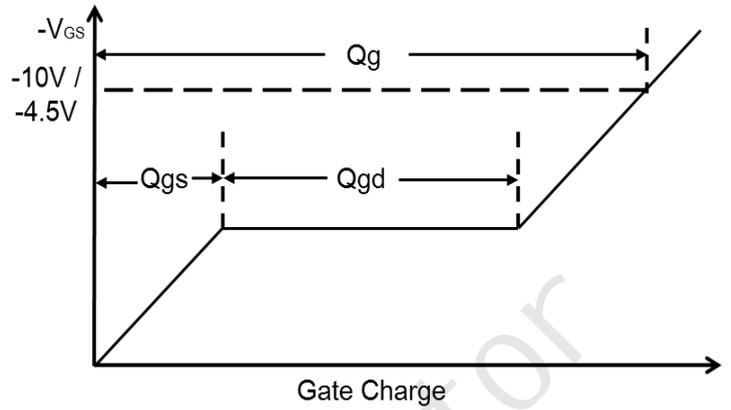


Fig.8 Gate Charge Waveform

JSMICRO Semi-conductor

**TO-252 Package Information**

