

Description

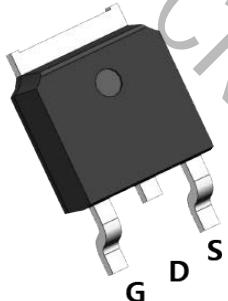
The JSM100N03 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

Application

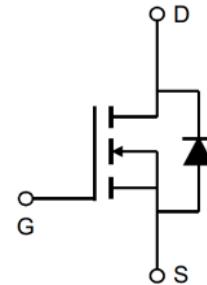
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

Features

- $V_{DS} = 30V, I_D = 100A$
- $R_{DS(ON)} : 5.5m\Omega @ V_{GS}=10V$
- Low gatecharge.
- Green device available.
- Advanced high cell density trench technology for ultra $R_{DS(ON)}$.
- Excellent package for good heat dissipation.



Marking and pin assignment



N-Channel MOSFET

Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	100	A
Drain Current-Continuous($T_c=100^\circ C$)	$I_D (100^\circ C)$	70	A
Pulsed Drain Current	I_{DM}	400	A
Maximum Power Dissipation	P_D	110	W
Single pulse avalanche energy ^(Note 5)	E_{AS}	350	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	1.36	°C/W
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Package Marking and Ordering Information

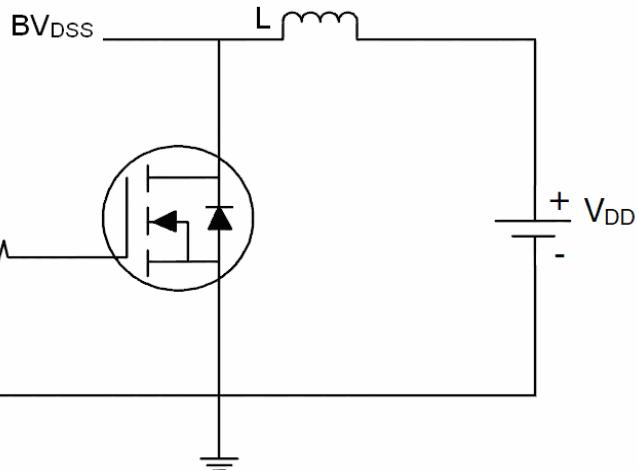
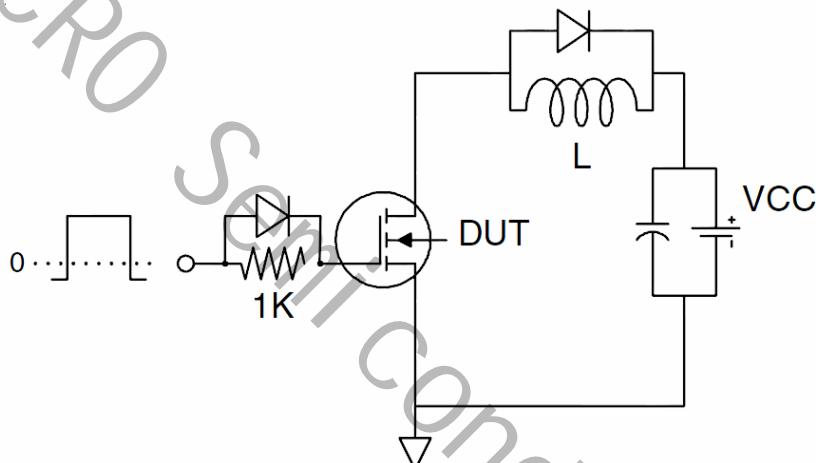
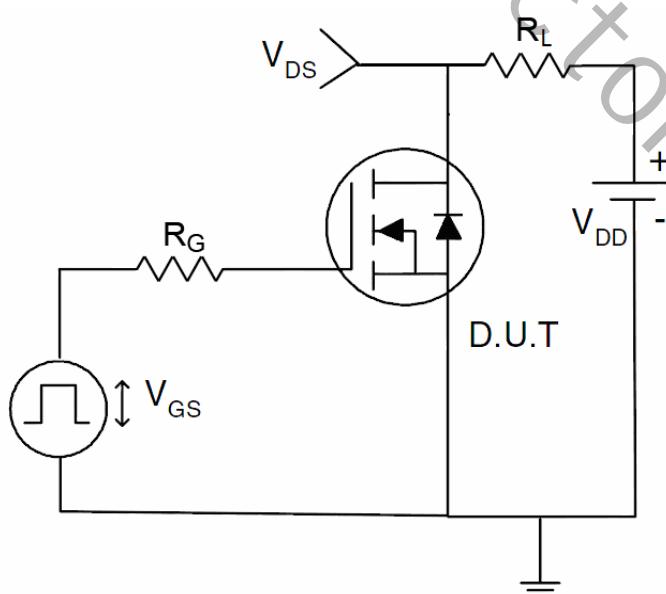
Part NO.	Marking	Package
JSM100N03	JSM100N03	TO-252

Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=30\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1	1.6	3	V
Drain-Source On-State Resistance	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=20\text{A}$	-	4.0	5.5	m
Forward Transconductance	g_{FS}	$V_{\text{DS}}=10\text{V}, I_{\text{D}}=20\text{A}$	50	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{iss}	$V_{\text{DS}}=25\text{V}, V_{\text{GS}}=0\text{V}, F=1.0\text{MHz}$		3400		PF
Output Capacitance	C_{oss}			356		PF
Reverse Transfer Capacitance	C_{rss}			308		PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}}=15\text{V}, I_{\text{D}}=60\text{A}$ $V_{\text{GS}}=4.5\text{V}, R_{\text{GEN}}=1.8$	-	11	-	nS
Turn-on Rise Time	t_r		-	160	-	nS
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$		-	25	-	nS
Turn-Off Fall Time	t_f		-	60	-	nS
Total Gate Charge	Q_g	$V_{\text{DS}}=15\text{V}, I_{\text{D}}=30\text{A}, V_{\text{GS}}=10\text{V}$		70		nC
Gate-Source Charge	Q_{gs}			8.8		nC
Gate-Drain Charge	Q_{gd}			16.3		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{\text{GS}}=0\text{V}, I_{\text{S}}=20\text{A}$	-	-	1.2	V
Diode Forward Current (Note 2)	I_{S}	-	-	-	100	A
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}, IF = 60\text{A}$ $di/dt = 100\text{A}/\mu\text{s}$ (Note 3)	-	56	-	nS
Reverse Recovery Charge	Q_{rr}		-	110	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_j=25^\circ\text{C}, V_{\text{DD}}=15\text{V}, V_{\text{G}}=10\text{V}, L=0.5\text{mH}, R_g=25$

Test circuit**1) E_{AS} test Circuits****2) Gate charge test Circuit:****3) Switch Time Test Circuit:**

Typical Electrical and Thermal Characteristics (Curves)

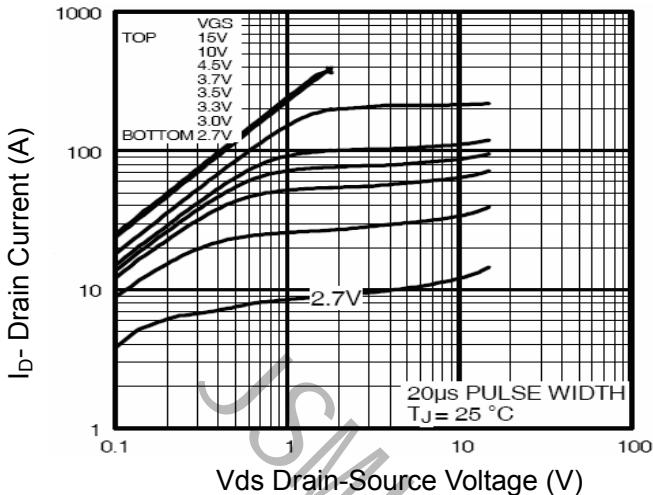


Figure 1 Output Characteristics

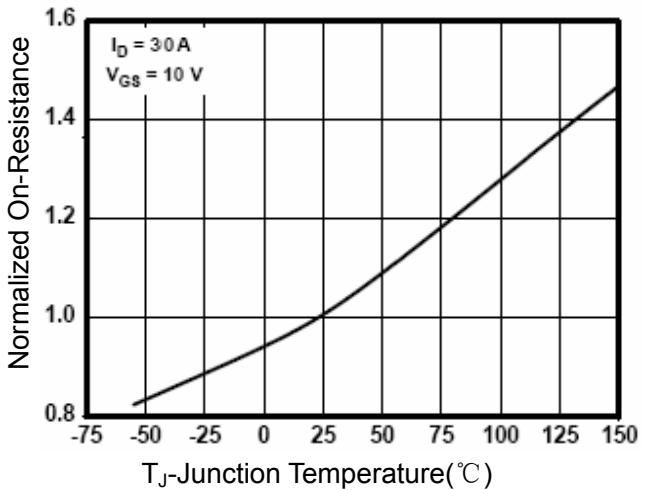


Figure 4 R_{DSON} -Junction Temperature

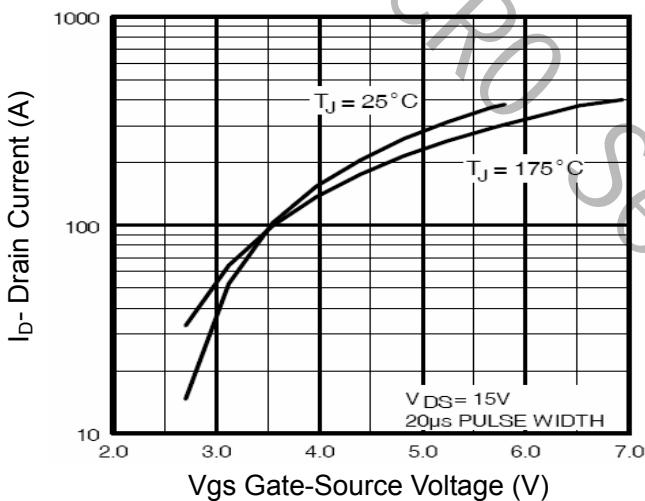


Figure 2 Transfer Characteristics

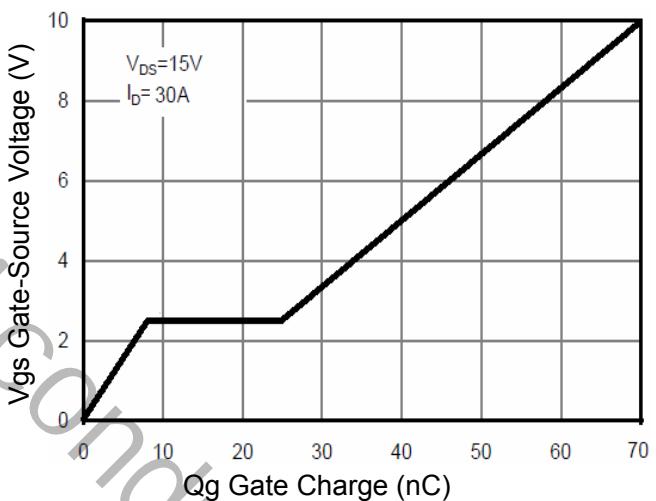


Figure 5 Gate Charge

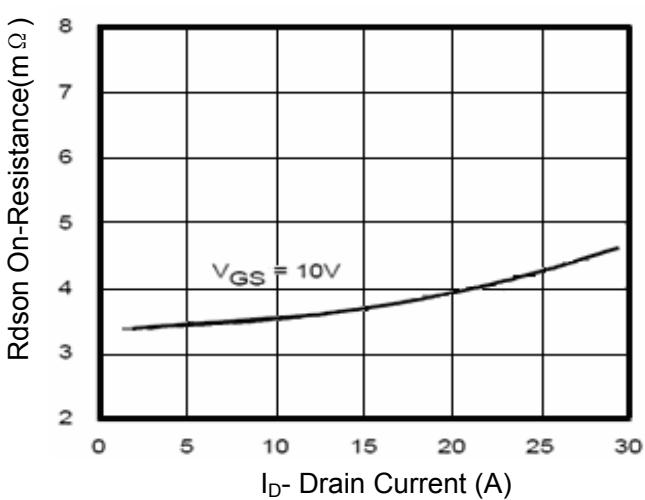


Figure 3 R_{DSON} - Drain Current

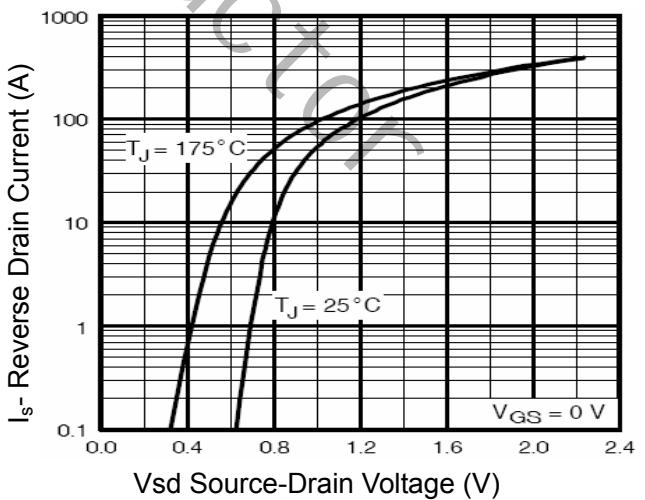
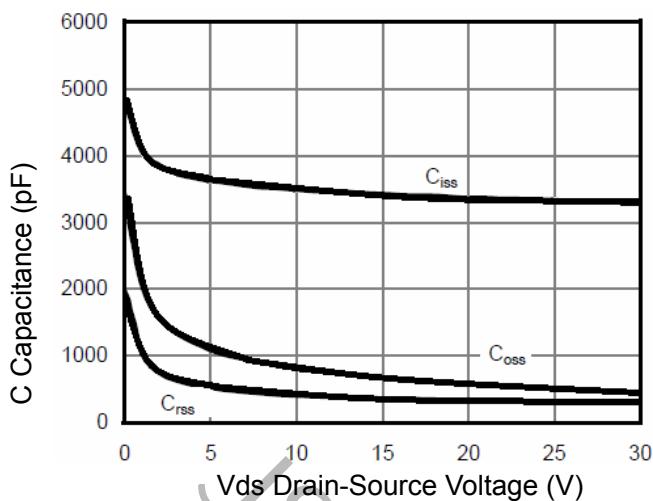
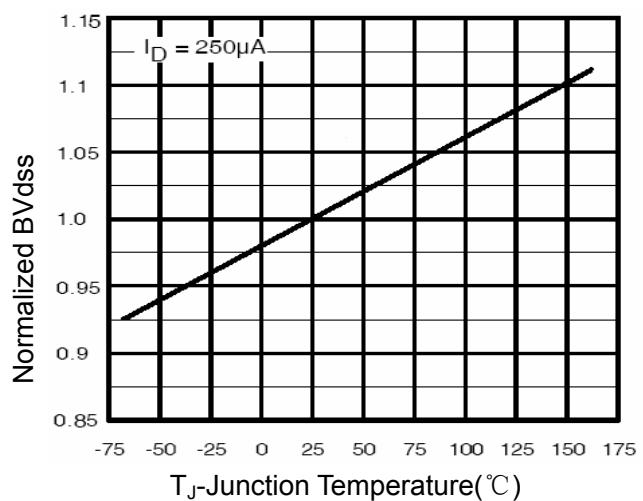
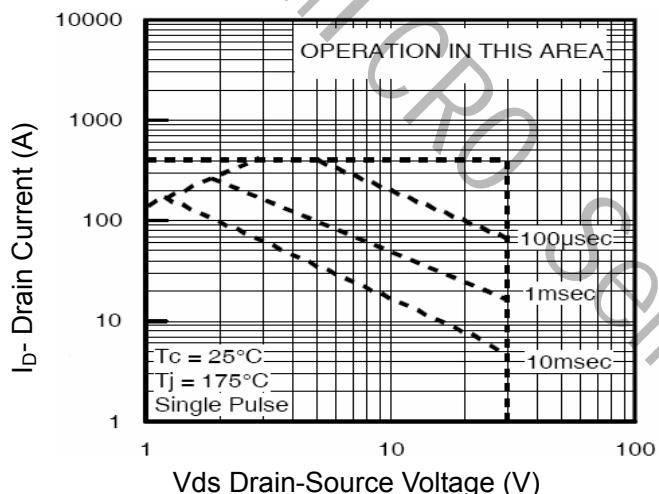
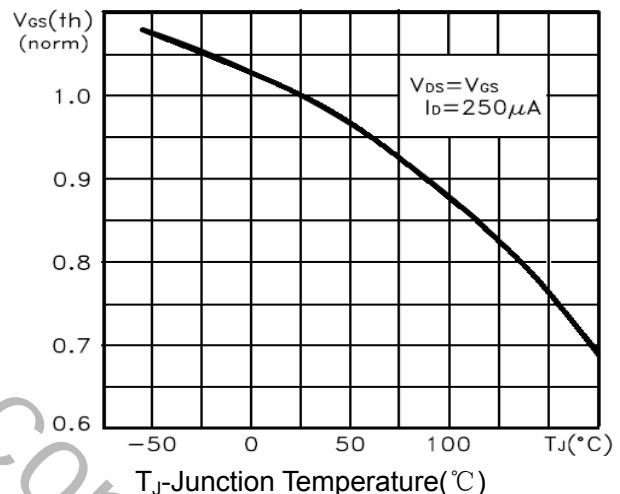
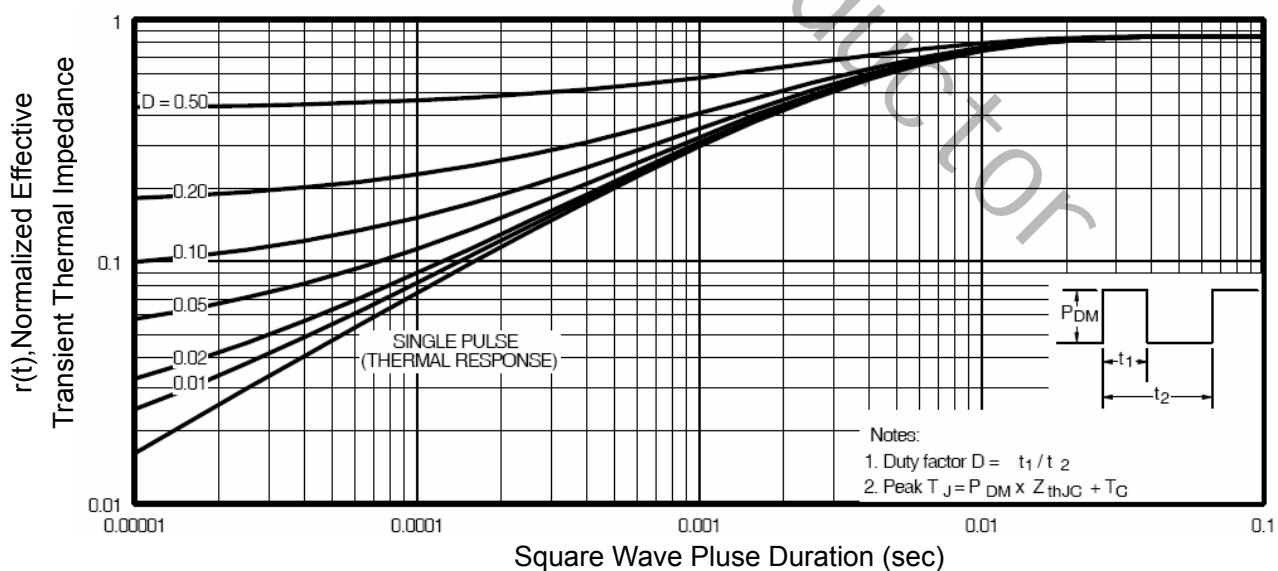


Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 BV_{DSS} vs Junction Temperature

Figure 8 Safe Operation Area

Figure 10 $V_{GS(th)}$ vs Junction Temperature

Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252 Package Information

